PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

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PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	12 JUL 1995
Applicant's or agent's file reference: TCOM1009(WO)	IMPORTANT NOTIFICATION

International application No.	International filing date *(day/month/year)*	Priority Date *(day/month/year)*
PCT/US93/12652	28 DECEMBER 1993	02 FEBRUARY 1993

Applicant
3COM CORPORATION

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US	Authorized officer
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Form PCT/IPEA/416 (July 1992)★

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference TCOM1009(WO)	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US93/12652	International filing date *(day/month/year)* 28 DECEMBER 1993	Priority date *(day/month/year)* 02 FEBRUARY 1993
International Patent Classification (IPC) or national classification and IPC IPC(6): G06F 13/24 and US Cl.: 395/275		
Applicant 3COM CORPORATION		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets.

   [X] This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 10 sheets.

3. This report contains indications relating to the following items:

   - I [X] Basis of the report
   - II [ ] Priority
   - III [ ] Non-establishment of report with regard to novelty, inventive step or industrial applicability
   - IV [ ] Lack of unity of invention
   - V [X] Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI [ ] Certain documents cited
   - VII [ ] Certain defects in the international application
   - VIII [X] Certain observations on the international application

Date of submission of the demand	Date of completion of this report
18 AUGUST 1994	19 JUNE 1995
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer CHRISTOPHER B SHIN Telephone No. (703) 305-9600

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US93/12652

I. Basis of the report

1. This report has been drawn on the basis of *(Substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments)*:

☐ the international application as originally filed.

☒ the description, pages (See Attached) , as originally filed.
pages _____ , filed with the demand.
pages _____ , filed with the letter of _____.
pages _____ , filed with the letter of _____.

☒ the claims, Nos. (See Attached) , as originally filed.
Nos. _____ , as amended under Article 19.
Nos. _____ , filed with the demand.
Nos. _____ , filed with the letter of _____.
Nos. _____ , filed with the letter of _____.

☒ the drawings, sheets/~~fig~~ (See Attached) , as originally filed.
sheets/~~fig~~ _____ , filed with the demand.
sheets/~~fig~~ _____ , filed with the letter of _____.
sheets/~~fig~~ _____ , filed with the letter of _____.

2. The amendments have resulted in the cancellation of:

☒ the description, pages NONE.

☒ the claims, Nos. NONE.

☒ the drawings, sheets/~~fig~~ NONE.

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the ~~Supplemental Box~~ Additional observations below (Rule 70.2(c)).

4. Additional observations, if necessary:

NONE

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims	1-30	YES
	Claims	NONE	NO
Inventive Step (IS)	Claims	8-9, 14-16, AND 18-21	YES
	Claims	1-7, 10-13, 17, AND 22-30	NO
Industrial Applicability (IA)	Claims	1-30	YES
	Claims	NONE	NO

2. CITATIONS AND EXPLANATIONS

I. Claims 1-7, 10-13, 17, and 22-30 lack an inventive step under PCT Article 33(3) as being obvious over Yasui et al. (5,161,228).

For claims 1-7, Yasui teaches, in figure 1, the basic claimed structure as follows:

Claims 1-7	Yasui (Fig 1)
- host	- (3)
- indication signal	- (INT0B-INT13B)
- first mask logic	- (11,12)
- first memory location	- (16,4)
- second mask logic	- (22a,22b)
- second memory location	- (26a,4)
- interrupt means	- (15,25a)
- indication/interrupt values	- content of (16,24a,4)

The main difference between the claimed structures and Yasui reference is that the reference does not expressly disclose the host system environment; however, the difference is an obvious design choice matter from the teachings of Yasui's system. As claimed, an interrupt managing/handling system is a basic and necessary part of any computer system, and a system or technique for notifying/indicating interrupts/conditions are well known and required by computer systems; as a result, one of ordinary skilled artisan can easily be motivated to utilize such well known required part of the system in the host oriented system. Therefore, it would have been obvious at the time the invention was made to one having ordinary skill in the art to utilize such well known technique, as taught by Akashi, in the claimed system for the reasons stated above.

For claims 10-13 and 17, Yasui teaches the claimed structure as follows:

Claims 10-13,17	Yasui (Fig 1)
- host	- (3)
- indication signals	- (INT0B-INT13B)
- indication mask logic	- (11,12)
- indication memory location	- (16,4)
- interrupt mask logic	- (22a,22b)
- interrupt memory location	- (26a,4)
- interrupt means	- (15,25a)

(Continued on Supplemental Sheet.)

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

I. Claims 1-17 are objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because the claims indefinite for the following reason(s):

a) In claim 1;

1) In lines 3 & 9, the phrases "capable of selectively masking" are vague and indefinite (i.e., it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.).

2) In line 8, it is unclear as to whether the second mask logic receives the "indication value" from the first location or the first logic.

3) In line 14, it is unclear as to whether the interrupt means responsive to the interrupt value from the second location or from the second logic.

4) In claim 1, it is unclear as to how the memory stored indication value & interrupt value are utilized by the claimed system in terms of generating an interrupt to the host, other than simply being stored in the memory locations.

b) In claim 10;

1) In lines 6, 9, & 15, the phrases "capable of selectively masking" are vague and indefinite as to whether the **selective masking** has **actually** been performed or not (i.e., it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.).

2) In line 9, it is unclear as to where the individual indication signal is received from. What is the relationship between the "plurality of indication signals" (line 5)and "individual signals" (line 9) and "subset of individual signals". If the individual signals are not received from the counter logic, it is unclear as to how the "counter mask logic" is utilized by the claimed system in terms of presenting interrupt signals.

c) In claim 12, "individual signal" lacks proper and clear antecedent basis (i.e., there are more than one individual signals).

d) Claims 14-17, due to the similarity between the claims, the unclarities of the claims 10-13 are similarly applied.

e) In claim 22;

1) In line 4, it is unclear as to whether the interface or host identifies the events.

2) In line 9, it is unclear as to what events are identified **from** the first indication signal; in addition, it is unclear as

(Continued on Supplemental Sheet.)

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

I. BASIS OF REPORT:

This report has been drawn on the basis of the description,
pages, 1-68, as originally filed.
pages, NONE, filed with the demand.
and additional amendments:
NONE

This report has been drawn on the basis of the claims,
numbers, NONE, as originally filed.
numbers, NONE, as amended under Article 19.
numbers, NONE, filed with the demand.
and additional amendments:
Claims 1-30, filed with the letter of 03 May 1995.

This report has been drawn on the basis of the drawings,
sheets, 1-18, as originally filed.
sheets, NONE, filed with the demand.
and additional amendments:
NONE

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):
- interrupt/indication values - content of (16,24a,4)

The main difference between the claimed invention and teachings of the reference is that the reference does not expressly disclose the limitation regarding the host interrupt service routine/subroutine for controlling the interrupt mask. However, such limitation is obvious from the teachings of Yasui because the Yasui reference does teach the "CPU 3" setting/writing mask data to the mask register 11 (See column 6, lines 43-59). Furthermore, having interrupt service routine or subroutine for controlling or making interrupt is a common knowledge at the time of the invention. Therefore, it would have been obvious at the time the invention was made to one having ordinary skilled in the art to utilize such well known common known knowledge (e.g., interrupt service routine/subroutine for controlling/making interrupt) for the well known purpose of controlling interrupt, as stated above.

For claims 22-30, due to the similarity between the claims, the teachings of the claims 1-7 and 10-13, 17 are similarly applied.

II. Claims 8-9, 14-16 and 18-21 meet the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach or fairly suggest the claimed combination details.

---------- NEW CITATIONS ----------
US, A, 5,161,228 (YASUI ET AL.) 03 NOVEMBER 1992, See entire document (figure 1).
US, A, 5,179,704 (JIBBE ET AL.) 12 JANUARY 1993, See entire document (figures 4-6).

VIII. CERTAIN OBSERVATIONS ON THE APPLICATION (Continued):

to how the stored first indication signal is utilized by the claimed system in terms generating interrupt to the host.

CLAIMS

What is claimed is:

1. An apparatus for managing an indication signal supplied by a source of indication signals to present an interrupt signal to a host, comprising:

a first mask logic for receiving the indication signal and capable of selectively masking at least a portion of the indication signal to output an indication value;

a first memory location, coupled to the first mask logic, for storing the indication value;

a second mask logic, coupled to the first memory location, for receiving the indication value and capable of selectively masking at least a portion of the indication value to output an interrupt value;

a second memory location, coupled to the second mask logic, for storing the interrupt value; and

interrupt means, coupled to the second memory location and responsive to the interrupt value, for generating the interrupt signal to the host.

2. The apparatus of Claim 1, wherein the first memory location is also coupled to the host for processing the indication value by the host.

3. The apparatus of Claim 1, wherein the second memory location is also coupled to the host for processing the interrupt value by the host.

4. The apparatus of Claim 1, wherein the first and second memory locations are coupled to the host for processing the indication value and the interrupt value by the host in response to an interrupt signal.

5. The apparatus of Claim 1, further comprising a first mask, coupled to the first mask logic, wherein the first mask logic is responsive to the first mask, and includes a first mask memory location, coupled to the host, the

first mask memory location responsive to a write by the host for storing the first mask.

6. The apparatus of Claim 1, further comprising a second mask, coupled to the second mask logic, wherein the second mask logic is responsive to the second mask, and includes a second mask memory location, coupled to the host, the second mask memory location responsive to a write by the host for storing the second mask.

7. The apparatus of Claim 1, wherein the host comprises a first condition and a second condition, the apparatus further comprising:

a first mask, including a first mask memory location, coupled to the host, the first mask memory location responsive to a write by the host during the first condition, for storing the first mask, and wherein the first mask logic is responsive to the first mask; and

a second mask, including a second mask memory location, coupled to the host, the second mask memory location responsive to a write by the host during the second condition, for storing the second mask, and wherein the second mask logic is responsive to the second mask.

8. The apparatus of Claim 5, wherein the first mask logic includes:

an AND gate having at least a first and second input and an output, the first input coupled to the indication signal, the second input coupled to the first mask memory location, and the output coupled to the first memory location for storing the indication value

9. The apparatus of Claim 6, wherein the second mask logic includes:

an AND gate having at least a first and a second input and an output, the first input coupled to the first memory location, the second input coupled to the second mask memory location, and the output coupled to the second memory location for storing the interrupt value.

10. An apparatus for managing a plurality of indication signals supplied by a source of indication signals to present an interrupt signal to a host having a host processor with an interrupt service routine and a host data bus, comprising:

counter mask logic for receiving the plurality of indication signals and capable of selectively masking at least a subset of the plurality of indication signals;

indication mask logic, coupled to the counter mask logic, for receiving individual indication signals and capable of selectively masking the individual indication signals to output an indication value;

an indication memory location, coupled to the indication mask logic, for storing the indication value;

interrupt mask logic, coupled to the indication memory location, for receiving at least a portion of the indication value and capable of selectively masking at least a portion of the indication value to output an interrupt value;

an interrupt memory location, coupled to the interrupt mask logic, for storing the interrupt value; and

interrupt means, coupled to the interrupt memory location and responsive to the interrupt value, for generating the interrupt signal on the host data bus to the host processor.

11. The apparatus of Claim 10, wherein the indication memory location and interrupt memory location are coupled to the host processor for processing the indication value and the interrupt value by the host processor during the interrupt service routine.

12. The apparatus of Claim 10, wherein the indication mask logic and interrupt mask logic include a first and second register, respectively, coupled to the host processor, selectively masking the individual indication signal and indication value responsive to a write by the host processor to the first or second register, respectively.

13. The apparatus of Claim 10, wherein the host includes host software having a subroutine and the counter mask logic includes:

means for masking the subset of the plurality of indication signals responsive to a host signal generated by the subroutine; and

means for unmasking the subset of the plurality of indication signals responsive to the host signal generated by the subroutine.

14. An apparatus for managing a plurality of indication signals supplied by a source of indication signals to present an interrupt signal to a host having a host processor with an interrupt service routine and a host data bus, comprising:

counter mask logic for receiving the plurality of indication signals and capable of selectively masking at least a subset of the plurality of indication signals;

indication mask logic, coupled to the counter mask logic, for receiving individual indication signals and capable of selectively masking the individual indication signals to output an indication value;

an indication memory location, coupled to the indication mask logic, for storing the indication value ;

interrupt mask logic, coupled to the indication memory location, for receiving at least a portion of the indication value and capable of selectively masking at least a portion of the indication value to output an interrupt value;

an interrupt memory location, coupled to the interrupt mask logic, for storing the interrupt value; and

interrupt means, coupled to the interrupt memory location and responsive to the interrupt value, for generating the interrupt signal on the host data bus to the host processor, wherein the host includes host software having a plurality of subroutines and the counter mask logic includes:

a counter memory location containing a counter value;

means for incrementing the counter value in the counter memory location responsive to a first host signal generated by at least a first subroutine;

means for decrementing the counter value in the counter memory location responsive to a second host signal generated by at least a second subroutine; and

means for masking the subset of the portion of the plurality of indication signals responsive to the counter value in the counter memory location.

15. The apparatus of Claim 14, wherein the counter memory comprises a plurality of memory cells, each memory cell coupled to an OR gate having an output signal masking the subset of the plurality of indication signals responsive to a counter memory value.

16. The apparatus of Claim 15, wherein the means for masking the subset of the plurality of indication signals includes a plurality of AND gates, individual AND gates having at least a first and second input and an output, the first input coupled to the subset of the plurality of indication signals and the second input coupled to the output signal of the OR gate masking at least the subset of the indication signal at the output of individual AND gates responsive to a counter memory value.

17. A network adapter for transferring data between a network transceiver coupled with a network, and a host system having a host processor, the network adapter generating a plurality of indication signals in response to network adapter events for management by the host processor to present an interrupt signal to the host processor, comprising:

counter mask logic for receiving the plurality of indication signals and capable of selectively masking at least a subset of the plurality of indication signals, the counter mask logic having a first register for selectively masking the subset of the plurality of indication signals responsive to the host processor writing to the first register;

indication mask logic, coupled to the counter mask logic, for receiving individual indication signals from among the portion of the plurality of indication signals and capable of selectively masking the individual indication signals to

output individual indication values, the indication mask logic having a second register for selectively masking the individual indication signals responsive to a write by the host processor to the second register;

an indication memory location, coupled to the indication mask logic, for storing the individual indication values and for reading by the host processor;

interrupt mask logic, coupled to the indication memory location, for receiving the individual indication values and capable of selectively masking individual indication values, the interrupt mask logic having a third register for selectively masking individual indication values to output an interrupt value responsive to a write by the host processor to the third register;

an interrupt memory location, coupled to the interrupt mask logic, for storing the interrupt value and for reading by the host processor; and

interrupt means, coupled to the interrupt memory location, for generating the interrupt signal to the host processor responsive to the interrupt value.

18. A network adapter for transferring data between a network transceiver coupled with a network, and a host system having a host processor, the network adapter generating a plurality of indication signals in response to network adapter events for management by the host processor to present an interrupt signal to the host processor, comprising:

counter mask logic for receiving the plurality of indication signals and capable of selectively masking at least a subset of the plurality of indication signals, the counter mask logic having a first register for selectively masking the subset of the plurality of indication signals responsive to the host processor writing to the first register;

indication mask logic, coupled to the counter mask logic, for receiving individual indication signals from among the portion of the plurality of indication signals and capable of selectively masking the individual indication signals to output individual indication values, the indication mask logic having a second register for selectively masking the individual indication signals responsive to a write by the host processor to the second register;

an indication memory location, coupled to the indication mask logic, for storing the individual indication values and for reading by the host processor;

interrupt mask logic, coupled to the indication memory location, for receiving the individual indication values and capable of selectively masking individual indication values, the interrupt mask logic having a third register for selectively masking individual indication values to output an interrupt value responsive to a write by the host processor to the third register;

an interrupt memory location, coupled to the interrupt mask logic, for storing the interrupt value and for reading by the host processor; and

interrupt means, coupled to the interrupt memory location, for generating the interrupt signal to the host processor responsive to the interrupt value, wherein the host includes host software having a plurality of subroutines and the counter mask logic includes:

means for incrementing a counter value in the first register responsive to a first host signal generated by at least a first subroutine; and

means for decrementing the counter value in the first register responsive to a second host signal generated by at least a second subroutine.

19. The apparatus of Claim 18, wherein the first register comprises a plurality of memory cells, each memory cell coupled to an OR gate having an output signal masking the subset of the plurality of indication signals responsive to the counter value.

20. The apparatus of Claim 18, wherein the counter value in the first register is between 0 and a positive number.

21. A network adapter for transferring data between a network transceiver, coupled with a network, and a host system having a host processor and host software subroutines, the network adapter generating a plurality of indication signals in response to the transferring of data for management by the host processor to present an interrupt signal to the host

processor, comprising:

counter mask logic for receiving the plurality of indication signals and capable of selectively masking at least a subset of the plurality of indication signals, the counter mask logic having a first register for selectively masking the subset of the plurality of indication signals responsive to the host processor writing to the first register during a host software subroutine;

indication mask logic, coupled to the counter mask logic, for receiving individual indication signals from among the plurality of indication signals and capable of selectively masking the individual indication signals to output individual indication values, the indication mask logic having a second register for selectively masking the individual indication signals responsive to a write by the host processor to the second register;

a first indication memory location, coupled to the indication mask logic, for storing the individual indication values representing high priority individual indication signals and for reading by the host processor during a host software subroutine;

a second indication memory location, coupled to the indication mask logic, for storing the individual indication values representing low priority individual indication signals and for reading by the host processor during a host software subroutine;

interrupt mask logic, coupled to the first and second indication memory locations, for selectively disabling individual indication values that were not disabled by the indicating mask logic, the interrupt mask logic having a third register selectively disabling individual indication values responsive to a write by the host processor to the third register;

a first interrupt memory location, coupled to the interrupt mask logic, for storing an interrupt value representing individual high priority indication values and for reading by the host processor;

a second interrupt memory location, coupled to the interrupt mask logic, for storing an interrupt value representing individual low priority indication values and for reading by the host processor; and

interrupt means, coupled to the first and second interrupt memory locations, for generating the interrupt signal to the host processor responsive to the interrupt value.

22. A method for managing transfer of signals from a network interface device to a host system, the signals indicating events caused or detected by the network interface device, comprising:

identifying events about which the host should have knowledge;

selectively masking at least a portion of the events with a first mask to output a first indication signal;

storing the first indication signal in a host accessible store in response to the first mask;

identifying events from the first indication signal to interrupt the host; and

selectively masking at least a portion of the first indication signal with a second mask to output a second indication signal to interrupt the host.

23. The method of Claim 22, further comprising:

generating a host interrupt signal in response to the second indication signal; and

supplying the host interrupt signal to the host.

24. The method of claim 22, further comprising:

dynamically altering the first and second masks in response to activity in the host.

25. A method of managing indication signals by a host processor, the indication signals generated from a network adapter in response to data transfer events occurring at the network adapter, comprising:

providing the indication signals along a portion of a data path between the network adapter and the host processor;

selectively masking at least a subset of the indication signals at a first mask, the first mask having a first mask pattern, to output a set of first masked signals;

selectively masking at least a subset of the first masked signals at a second mask, the second mask having a second mask pattern, to output a set of second masked signals; and

presenting a host interrupt signal to the host processor in response to the indication signals, the first mask, and the second mask.

26. The method of Claim 25, further comprising:

controlling, by the host processor, the first mask pattern and the second mask pattern of the first mask and the second mask, respectively, to control the selective masking steps at the first mask and the second mask.

27. The method of Claim 26, further comprising:

storing the set of first masked signals and the set of second masked signals at a memory location.

28. The method of Claim 27, wherein the step of storing comprises:

storing the set of first masked signals at a first memory location; and

storing the set of second masked signals at a second memory location.

29. The method of Claim 27, wherein the step of presenting the host interrupt signal to the host processor is accomplished by the host processor reading the memory location.

30. The method of Claim 26, including generating the host interrupt signal in response to the second masked signals and reading the first masked signals to learn of events not subject of host interrupt signals.